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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,938	10/31/2001	William B. Connors	10007153-1	4722

7590 11/10/2005  
HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER
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NGUYEN, LAM S

ART UNIT	PAPER NUMBER
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2853

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/003,938	<b>Applicant(s)</b> CONNORS ET AL.	
	<b>Examiner</b> LAM S. NGUYEN	<b>Art Unit</b> 2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2005.
- 2a) ☒ This action is FINAL.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 2-9, 17-20, 22-25, 27-30 and 36-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-9, 17-20, 22-25, 27-30 and 36-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### Response to Declaration Under § 1.131

The declaration filed on 08/25/2005 under 37 CFR 1.131 has been considered but is ineffective to overcome the Feinn et al. reference (US 6260952).

The evidence submitted to show the conception date (09/01/2000) of the current claimed invention is insufficient to establish a reduction to practice of the invention in this country of a NAFTA or WTO member country prior to the effective date, which is the effective US filing date (04/22/1999), of the Feinn et al. reference. (*MPEP 715, III < REFERENCE DATE TO BE OVERCOME defines that "The date to be overcome under 37 CFR 1.131 is the effective date of the reference" and MPEP 2136.03[R-2], V. DATE OF CONCEPTION OR REDUCTION TO PRACTICE defines that "the effective date of the reference as prior art is its filing date in the United States"*).

As a result, the claim rejection based on the Feinn et al. reference is maintained as follows:

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 2, 3-9, 17-20, 22-25, 27-30, 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasamoto et al. (US 6056391) in view of Feinn et al. (US 6260952).

**Referring to claims 2, 17, 20, 22, 27, 36, 39-40:**

Kasamoto et al. discloses a printhead having a circuit with plural resistors and a power source, comprising:

a metal stack formed within the circuit and comprised of a first/bottom metal layer (*FIG. 1c, element 1110c-b*) comprising a power bus/conductive trace coupled to the power source (*FIG. 1C: The layers 1110c-b are connected to a power source*) and a second/top metal layer comprising a top conductive layer portion and a bottom layer portion (*FIG. 1c, elements 1110a, 1103*), wherein the bottom layer portion has a portion that comprises the resistors (*FIG. 1c, element 1102*) (**Referring to claim 21, 26**), and

at least one power via (*FIG. 1c, element 1105*) formed within the circuit as an interface between the first metal layer and the second metal layer, wherein, at the power via the second metal layer comprises a separation barrier (*FIG. 1c: The portion of layer 1103 in the area 1105, that is sandwiched between layer 1110c and layer 1110d*) located adjacent the first metal layer (*FIG. 1c, element 1110c*) and between the at least one resistor (*FIG. 1c, element 1102*) of the plural resistors and the power bus (*FIG. 1C: The power is supplied to resistor 1102 relatively through layer 1110c and the separation barrier*), and wherein the second metal layer is connected to the first conductive metal layer portion at the plurality of electrical connection portions (*FIG. 1c, element 1105: The portion of layer 1103 at area 1105*) (**Referring to claims 2, 21-23, 26, 38**),

wherein, at the via, the first metal layer (*FIG. 1C, layer 1110c*) is separated from the top conductive layer portion (*FIG. 1C, layer 1110d*) by the electrical connection portion of the bottom layer portion (*FIG. 1C, layer 1103*) (**Referring to claim 22**).

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Kasamoto et al. does not disclose a controller/FET bus that is connected to the at least one resistor at a controller/FET via, wherein, at the controller/FET via, the second metal layer comprises a separation barrier located adjacent the first metal layer and between the at least one resistor of the plural resistors and the controller/FET bus. In other words, Kasamoto et al. does not disclose a controller via that is in the same structure with the power via and connects the at least one resistor to a controller/FET bus.

Fein et al. discloses an ink jet printhead having a plurality of resistors for causing ink ejection when applied by an electrical power, wherein each of the resistors is connected to a power/control source through two traces, wherein the traces are dropped through similar-in-structure vias (*Abstract and column 5, lines 59-65*).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the printhead disclosed by Kasamoto et al. to connect the other end of the at least resistor to a control source through a via that is similar to the power vis as disclosed by Feinn et al. The motivation for doing so would have been to reduce the likelihood of electrical shorting as taught by Feinn et al. (*column 2, lines 60-65*).

- **Kasamoto et al. also discloses the following claimed invention:**

**Referring to claims 3, 24, 29:** (*Claim 24 is assumed to be dependent from claim 22*) wherein the circuit is a thin film circuit and the first metal layer is comprised of Aluminum Copper Silicon (*column 5, lines 35-42: "Cu Al-Si alloy"*).

**Referring to claims 6, 19:** connecting a power bus to the at least one thin film resistor with a power via (*FIG. 1C: The power is supplied to thin film resistor 1102 relatively through the power via 1105*), and wherein ink corrosion is terminated by the separation barrier at the

power/controller via (*column 2, lines 30-45*).

**Referring to claims 7-8:** wherein the plural resistors comprise a set of resistors, wherein for the set of resistors, power is routed from the power bus through a plurality of corresponding power/controller vias to each resistor of the set of resistors (*FIG. 1c: The printhead has a plurality of resistors 1102, wherein each resistor 1102 is provided electrical energy through the connection of the electrodes 1110d and 1110a to a corresponding power/controller via*).

**Referring to claim 9:** wherein each resistor of the plural resistors is associated with at least one power via that separates metal of the resistor from the power bus (*FIG. 1C: The portion 1105 of the layer 1103 separates the metal layer 1110d to the layer 1110b-c*).

**Referring to claims 4-5, 25, 30:** (*claim 25 is assumed to be dependent from claim 22*) wherein the second metal layer is comprised of Aluminum and at least one of Tantalum Aluminum, Tungsten Silicon Nitride, or Tantalum Nitride which provides corrosion resistance and connects the Aluminum to the power bus (*column 9, lines 1-3*), wherein a first portion of the Tantalum Aluminum comprises the corresponding at least one of the resistor and a second portion of the Tantalum Aluminum connects the corresponding at least one of the resistor to the power bus (*FIG. 1C*).

**Referring to claim 32:** a non-metal layer overlying the first metal layer and comprising a via (*FIG. 1c, element 1112: The non-metal layer 1112 comprises the via 1105*), wherein the first metal layer is electrically connected to the electrical connection portion of the bottom layer portion at the via (*FIG. 1c: The first metal layer 1110c is electrically connected to the bottom layer 1103 at the via 1105*), wherein the first metal layer is electrically connected to the first electrical connection portion at the first via and the first metal layer is electrically connected to

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the second electrical connection portion at the second via (*Fig. 1B-C: The first metal layer 1110c is connected to each of the resistor 1102 through a corresponding via 1105*).

**Referring to claims 18, 28, 36-37, 39-40:** wherein the second conductive metal layer comprises a corrosion-resistive layer portion (*FIG. 1C and column 9, lines 1-4: Layer 1103 is a 600Å thick tantalum nitride layer which is a corrosion-resistant material*).

### ***Response to Arguments***

Applicant's arguments filed 08/25/2005 have been fully considered but they are not persuasive.

The applicant argued that since the declaration under 37 C.F.R. § 1.131 establishes the conception date (09/01/2000) that is prior the publication date of the Feinn reference (07/17/2001), the Feinn reference is available as a reference under 35 U.S.C. § 102(e), the Feinn reference, thus, is not available as a reference under 35 U.S.C. § 103(a) due to common assignment. In response, the examiner cites that "For 35 U.S.C. § 102(a) to apply, the reference must have a publication date earlier in time the effective filing date of the application, and must not be applicant's own work" (*MPEP 706.02(b) C. <35 U.S.C. § 102(a)*). In this case, since the Feinn reference was published (on 07/17/2001) prior the effective filing date of the application (10/31/2001) and Feinn's invention is not the applicant's own work, the Feinn reference is available as a reference under 35 U.S.C. § 102(a) and also available as a reference under 35 U.S.C. § 103(a) even though the Feinn reference and the application are owned by the same assignee. As a result, the 103 rejection based on the Feinn reference is maintained as above.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S. NGUYEN whose telephone number is (571)272-2151. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEPHEN D. MEIER can be reached on (571)272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR



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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN

11/02/2005



HAI PHAM  
PRIMARY EXAMINER